What is claimed is:

1. An IC chip for reading an image, comprising:

a plurality of image reading photoelectric conversion elements

a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements;

a first signal selection circuit for sequentially selecting the plurality of first transistors;

a plurality of dummy photoelectric conversion elements arranged respectively near the image reading photoelectric conversion elements and shielded from light;

a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements;

a second signal selection circuit for sequentially selecting the plurality of second transistors; and

an output circuit for processing the first and second photoelectric conversion signals and then outputting a resulting signal,

wherein the output circuit outputs a difference between the first and second photoelectric conversion signals to correct the first photoelectric conversion signal.

2. An IC chip for reading an image, comprising:

a plurality of first processing sections, each comprising:

a plurality of image reading photoelectric conversion elements;

a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements;

a first signal selection circuit for sequentially selecting the plurality of first transistors; and

a first signal output line by way of which the first photoelectric conversion signal is transmitted,

wherein provision of the plurality of first processing sections reduces a total resistance and a total capacitance of the first signal output lines provided within the first processing sections, reduces a total parasitic capacitance of the first transistors connected to the first signal output lines, and thereby permits the image reading device to operate at a higher operation speed.

3. An IC chip for reading an image as claimed in claim 2, further comprising:

a dummy photoelectric conversion element shielded from light; and

an output circuit for outputting a difference between the first photoelectric conversion signal and a second photoelectric conversion signal read from the dummy photoelectric conversion element,

wherein the output circuit corrects the first photoelectric conversion signal.

4. An IC chip for reading an image, comprising:

a plurality of first processing sections, each comprising:

a plurality of image reading photoelectric conversion elements;

a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements;

a first signal selection circuit for sequentially selecting the plurality of

first transistors; and

a first signal output line by way of which the first photoelectric conversion signal is transmitted;

a plurality of second processing sections provided so as to pair respectively with the first processing sections, the second processing sections each comprising:

a plurality of dummy photoelectric conversion elements arranged respectively near the image reading photoelectric conversion elements and shielded from light;

a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements;

a second signal selection circuit for sequentially selecting the plurality of second transistors; and

a second signal output line by way of which the second photoelectric conversion signal is transmitted;

an output circuit for processing the first and second photoelectric conversion signals and then outputting a resulting signal; and

a signal output line switching circuit for selecting the first and second signal output lines and connecting the selected first and second signal output lines to the output circuit,

wherein the output circuit outputs a difference between the first and second photoelectric conversion signals to correct the first photoelectric conversion signal.

5. An image reading device comprising:

one or more IC chips, each comprising:

a plurality of image reading photoelectric conversion elements;

a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements;

a first signal selection circuit for sequentially selecting the plurality of first transistors;

a plurality of dummy photoelectric conversion elements arranged respectively near the image reading photoelectric conversion elements and shielded from light;

a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements;

a second signal selection circuit for sequentially selecting the plurality of second transistors;

an output circuit for outputting a difference between the first and second photoelectric conversion signals as a corrected first photoelectric conversion signal;

a trigger signal input terminal by way of which a signal for sequentially scanning an image being read is fed in from an IC chip in a previous stage;

a trigger signal output terminal by way of which a signal for sequentially scanning the image being read is fed out to an IC chip in a following stage;

a clock input terminal by way of which a clock is fed in; and

a reference voltage input terminal by way of which a reference voltage for the output circuit is fed in; and

an A/D converter for converting a signal output from the output circuit into a digital signal,

wherein said one or more IC chips each start scanning the image being read on receiving an input signal at the trigger input terminal thereof, and, on completion of the scanning, outputs, at the trigger output terminal thereof, a signal for continuing sequential scanning to the IC chip in the following stage.

6. An image reading device comprising:

one or more IC chips, each comprising:

a plurality of processing sections, each comprising:

a plurality of image reading photoelectric conversion elements;

a plurality of transistors for reading a photoelectric conversion signal from the image reading photoelectric conversion elements;

a signal selection circuit for sequentially selecting the plurality of transistors;

a signal output line by way of which the photoelectric conversion signal is transmitted;

a trigger signal input terminal by way of which a signal for sequentially scanning an image being read is fed in from an IC chip in a previous stage;

a trigger signal output terminal by way of which a signal for sequentially scanning the image being read is fed out to an IC chip in a following stage; and

a clock input terminal by way of which a clock is fed in;

wherein said one or more IC chips each start scanning the image being read on receiving an input signal at the trigger input terminal thereof, and, on completion of the scanning, outputs, at the trigger output terminal thereof, a signal for continuing sequential scanning to the IC chip in the following stage.

7. An image reading device as claimed in claim 6, wherein the IC chips each further comprise:

a dummy photoelectric conversion element shielded from light;

an output circuit for outputting a difference between the photoelectric conversion signal and a signal read from the dummy photoelectric conversion element,

wherein the output circuit corrects the photoelectric conversion signal.

8. An image reading device comprising:

one or more IC chips, each comprising:

a plurality of first processing sections, each comprising:

a plurality of image reading photoelectric conversion elements;

a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements;

a first signal selection circuit for sequentially selecting the plurality of first transistors; and

a first signal output line by way of which the first photoelectric conversion signal is transmitted;

a plurality of second processing sections provided so as to pair

respectively with the first processing sections, the second processing sections each comprising:

a plurality of dummy photoelectric conversion elements arranged respectively near the image reading photoelectric conversion elements and shielded from light;

a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements;

a second signal selection circuit for sequentially selecting the plurality of second transistors; and

a second signal output line by way of which the second photoelectric conversion signal is transmitted;

an output circuit for outputting a difference between the first and second photoelectric conversion signals as a corrected first photoelectric conversion signal;

a signal output line switching circuit for selecting the first and second signal output lines and connecting the selected first and second signal output lines to the output circuit;

a trigger signal input terminal by way of which a signal for sequentially scanning an image being read is fed in from an IC chip in a previous stage;

a trigger signal output terminal by way of which a signal for sequentially scanning the image being read is fed out to an IC chip in a following stage; and

a clock input terminal by way of which a clock is fed in;

an A/D converter for converting a signal output from the output circuit into a digital signal,

wherein said one or more IC chips each start scanning the image being read on receiving an input signal at the trigger input terminal thereof, and, on completion of the scanning, outputs, at the trigger output terminal thereof, a signal for continuing sequential scanning to the IC chip in the following stage.